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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,269	05/25/2001	Sasan Cyrusian	10808/27	5524

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/866,269	CYRUSIAN, SASAN	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5-14 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-14 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *20-23* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 02-01-05. Applicant's arguments with respect to references Du (USP. 5,568,099) and Johnson (5,994,939) 3have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remained rejected under Du.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2, 7-9, 10-14 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Du (US Pat. 5,568,099).

Regarding claim 2, figures 11 and 15 shows a delay lines comprising at least two four-transistor delay units, comprising: a first amplifier (4910, 4920) a second amplifier (4930, 4940). The differential inputs are signals (pi-1) and (ni-1). Signal (Vcnt') is the "supply voltage and control voltage".

Regarding claims 7, 8, 9 and 11, figures 11 and 15 shows a voltage-controlled oscillator comprising a first delay unit (4500-1), a second delay unit (4500-k) Note that the number of delay units in figure can be two. The structure of each unit is shown in figure 15. (Vcnt') is the control input and power supply for the amplifiers. The first amplifiers comprise PMOS transistors and the second amplifiers comprise NMOS transistors. The voltage (Vcnt') is a positive voltage (Vdd) and the ground is coupled to the second amplifiers.

Regarding claims 10 and 12, the oscillator further comprises additional delay unit (fig. 11).

Regarding claims 13, 14, 17 and 19, the output terminals are (no-1), (po-1). The interconnection is shown in figure 15. The first amplifiers comprise PMOS transistors and the second amplifiers comprise NMOS transistors. The additional delays and their connections are shown in figure 11.

Regarding claim 18, figure 2 of Du shows the charge pump (160) and the buffer (180). Note that loop filter (180) is a buffer between the charge pump and the VCO (200).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Du (US Pat. 5,568,099) in view of Johnson et al. (US Pat. 5,994,939).

Regarding claim 3, figure 15 of DU includes all the limitation of claim 3 except for the fifth and sixth transistors. Figure 4 of Johnson shows a differential amplifier comprising loads having two transistors connected in parallel for reducing the load resistance of the circuit. As a result, the current flow increases and the switching speed increases. Therefore, it would have been obvious to those skilled in the art to implement additional transistors taught by Johnson, in parallel, to the load transistors (4910) and (4920) for improving the speed of the circuit.

Regarding claims 5 and 6, figure 15 of DU includes all the limitation of claim 3 except for the values W/L of the NMOS and PMOS transistors. However, it is old and well known in the art that when W/L ratio increases, the resistance of the transistor decreases. Therefore, it would have been obvious to those skilled in the art to increase the W/L values of the PMOS transistors to a value larger than the W/L value of The NMOS transistors for reducing the load resistance thus, the speed of the circuit increases. Figure 11 shows a plurality of four-transistor delay circuit.

Response to Arguments

In the Remarks, page 13, the applicant argues that " Du required elements that are not present in the claim, inccluding the "clipper" transistor and its voltage source". That is true. The clipper transistor ((4950) in figure 15 of Du provides more control of the delay cell (col.10, lines 64-67). However in claim 2, The applicant recites that "A delay line ***comprising*** at least two four-transistor delay units connected in series, a four-transistor delay unit, ***comprising***: ..." . According to the language of the claim ***(comprising)***, the claim circuit can have more elements than the number of recited elements. Thus, the circuits of figures 11 and 15 of Du **comprise** all the elements of the circuit of claim 2. The applicant is suggested to narrow the scope of claim 2 in order to overcome the prior art by replacing "**comprising**" with "**consisting**". In page 14, the applicant argues that : Du does not teach or suggest the four transistor delay unit of the present application. As discussed above, figure 15 of Du does teach or suggest the four transistor delay unit of the present application. In page 14, the applicant argue that the combination of Johnson and DU is improper. Du shows a delay cell having single load transistors. Johnson shows a delay cell having loads ***comprising*** fifth and sixth transistors for **reducing the load resistance of the circuit** thus, the switching speed increases. Therefore, the 103 (a) rejection using the combination of Du and Johnson is proper. In page 14, the applicant argues that the delay cell of Johnson **comprises** eighteen transistors, load capacitor etc... The circuit of Johnson does teach loads comprising pair of transistors connected in parallel for ***reducing the load resistance and for increasing the switching speed*** (col. 4, lines 20-43). Thus the replacement of the load of the circuit of Du with the load of the circuit of Johnson does ***improve the performance of the circuit of Du.*** The Applicant id reminded that the previous office action did not replace the whole circuit of Du with the whole circuit of Johnson comprising 18 transistors. Only the ***loads*** of Du is replaced with the ***loads*** of Johnson for improving the functioning of the circuit of DU.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
04-04-05

TUAN T. LAM
PRIMARY EXAMINER